Claims

[c1] 1. A first-in-first-out semiconductor memory with error correction code function, comprising:
an error correction code encoder unit for receiving an input data and generating a check code according to the input data;
a first-in-first-out memory circuit for holding the input data and the check code and outputting the input data and the check code according to the first write-in first read-out rule; and
an error correction code decoder unit coupled to the first-in-first-out memory circuit for finding error bits according to the input data and the check code such that if an error bit is found and if the error byte is within a correctable byte error range, the decoder unit outputs a corrected input data.

[c2] 2. The first-in-first-out memory of claim 1, wherein the first-in-first-out memory circuit further includes:
a memory unit for holding input data and check codes;
a write control unit coupled to the memory unit, wherein the write control unit has a pointer for controlling the write-in sequence of the memory addresses of the input data and the check codes;
a read control unit coupled to the memory unit, wherein the read control unit has a pointer for controlling the read-out sequence of the memory addresses of the input data and the check codes; and
a flag logic unit coupled to the write control unit and the read control unit for setting up a memory full flag and a memory empty flag according to the value the write pointer and the read pointer.

[c3] 3. The first-in-first-out memory of claim 1, wherein the memory unit further includes regular memory and redundant memory.

[c4] 4. The first-in-first-out memory of claim 1, wherein the memory further includes a setting circuit for enabling or disabling the error correction code function in the first-in-first-out memory.

[c5] 5. The first-in-first-out memory of claim 4, wherein the setting circuit is constructed using an inverter and a multiplexer.

[c6] 6. The first-in-first-out memory of claim 1, wherein the correctable byte is one error bit.

[c7] 7. The first-in-first-out memory of claim 1, wherein the error correction code decoder unit is capable of finding two error bits in an error byte.